UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,592	10/27/2003	Eric Pihet	WMP-IFT-808	3500

27346 7590 06/09/2009

LERNER GREENBERG STEMER LLP
FOR INFINEON TECHNOLOGIES AG
P.O. BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
PATEL, KAMINI B	

ART UNIT	PAPER NUMBER
2114	

MAIL DATE	DELIVERY MODE
06/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,592	PIHET, ERIC	
	Examiner	Art Unit	
	KAMINI PATEL	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-28 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-28,30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to RCE filed on 04/15/2009, in which, Claims 12, 18 and 30 are amended.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/15/2009 has been entered.

Response to the arguments

3. Applicant's arguments with respect to claims 12-28, 30 have been fully considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claim 12-22, 25-28, 30*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Eisele et al. (U. S. Patent No. 6,034,995 referred herein after Eisele) in view of Williamson (U. S. Patent No. 5,124,990).

As per claim 12, Eisele discloses: a method for checking for line faults in a bus system having at least two bus subscribers connected to a data bus for data communication between the subscribers, the data bus having at least two bus lines, which comprises: (Eisele, fig. 1, col. 5, lines 57-64, "FIG. 1 shows diagrammatically three stations 1, 2 and 3 which are interconnected via three lines 11, 12 and 13.") where stations can be the "bus Subscribers" and lines 11,12, 13 can be "bus lines" as claimed;

configuring the bus subscribers with switches for placing the subscribers in a recessive state and a dominant state; (Eisele, col. 6, lines 17-21, "on the lines 11 and 12 in the case of open switches 6 and 7, therefore, will be referred to as the recessive state hereinafter and the state in the case of closed switches 6 and 7 as the dominant state.", where switches are used to place bus subscribers in recessive or dominant state as claimed);

making available an internal high potential and an internal low potential in the bus subscribers; (Eisele, col. 6, lines 15-16, "the line 11 carries a high potential and the line 12 carries a low potential.");

carrying out a check for line faults by comparing of voltage levels on the bus lines with threshold values related to one of an internal high level and an internal low level of the bus subscriber. (Eisele, fig. 2, col. 6, lines 28-51, "The line 11 is also connected to a comparator 22 which compares the potential on this line with a threshold value which is valued, taking into account tolerances, between the dominant and the recessive potential on the line 11. The comparator 22 generates a high signal on the line 32 if the potential on the line 11 exceeds the threshold value.").

Eisele does not specifically discloses ***a check for a line fault only when the at least one of the said bus subscribers is placed in said dominant state by said switching state of said switches;***

However, Williamson discloses the above claim limitations, (Fig. 6, element 614, 615, Col. 5, lines 1-9, where first and second pinned fault detection means checks for fault (short circuit) in the dominant state);

Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Williamson's diagnostic method to Eisele's teaching because one of the ordinary skill in the art would have been motivated to provide fault tolerant serial communications in a network (Williamson, Col. 2, lines 26-27).

As per claim 13, claim 12 is incorporated and Eisele further comprises: providing a supply voltage referenced to an internal reference ground potential in the bus subscribers, the threshold values being greater than the supply voltage; and (Eisele, fig. 1, col. 5, lines 66-67, col. 6, lines 1-3, "The line 11 is connected to ground via a resistor 14 and a switch. The line 12 is connected, via a resistor 15 and a further switch, to the operating voltage Vc which is derived from the supply voltage on the line 13 in the station.", col. 14, lines 1-13, "the line 11 carries the potential of the supply voltage;..... the line 11 carries a potential below said threshold voltage") where station can be "the bus subscriber" as claimed.

identifying a fault when one of the voltage levels on the bus lines is greater than the respective threshold value. (Eisele, col. 2, line 28-29, col. 1, lines 65-67, col. 2, lines 1-9, "comparator which is coupled to both lines in order to subtract the potential on the first line from the potential on the second line and to output an output signal of a first value via a first comparator output if the difference formed by the subtraction exceeds a first threshold value,") where voltage difference of two potentials can be "one of the voltage level on the bus line" as claimed and when the difference exceeds the threshold voltage, fault is identified as claimed.

As per claim 14, claim 13 is incorporated and Eisele further comprises

identifying a fault when one of the voltage levels on the bus lines is greater than the respective threshold value during a predetermined number of successive dominant states of the bus subscriber carrying out the fault identification. . (Eisele, col. 1, lines 65-67, col. 2, lines 1-9, col. 14, lines 14-36, "the line 12 carries the potential of the supply voltage which is detected by the comparator 25, also having a threshold voltage of 7.3 V with respect to ground……..one of the two lines carries a dominant signal … for a predetermined period of time").

As per claim 15, claim 12 is incorporated and Eisele further comprises: comparing the voltage levels on the data lines with one another for detection of transmitted data; and upon detection of a fault on one of the data lines, carrying out detection of transmitted data by comparing the voltage level on the other one of the data lines with a threshold value related to one of the internal high potential and the internal low potential. (Eisele, col. 2, lines 10-27, "a comparator which forms not only the difference between the potentials on the two lines but also compares this difference with a given first threshold value, the transmitted data signal..... each line is connected to a low potential or a high potential via a resistor") where one of the two lines interrupted means "fault detected" as claimed.

Claim 16 has similar limitations as claim 13 and claim 15 and therefore is

rejected under the same reasons set forth in rejection of claim 13 and claim 15 above.

Claim 17 has similar limitations as claim 15 and claim 14 and therefore is rejected under the same reasons set forth in rejections of claim 14 and claim 15 above.

As per claim 18, a bus system, comprising:

a data bus having at least two bus lines; and (Eisele, fig 1, bus lines 11, 12 and 13, col. 5, lines 58-60, "three lines 11, 12 and 13");

at least two bus subscribers coupled to said data bus for serial data transfer of binary data between said bus subscribers, at least one of said bus subscribers having: (Eisele, fig 1, stations 1, 2 and 3, col. 3, lines 2-5, col. 5, lines 58-64, "three stations 1, 2 and 3 which are interconnected via three lines 11, 12 and 13....the data is transmitted") where station can be "bus subscriber" as claimed;

at least one control unit; (Eisele, fig 1, element 5, col. 6, lines 5-15, "the station 2 comprises a control device 5") where control device can be "control unit" as claimed;

Switches for assuming a switching state placing the one of said bus subscribers in a dominant state; (Eisele, col. 6, lines 17-21, "the state in the case of closed switches 6 and 7 as the dominant state.", where switches are

used to place bus subscribers in recessive or dominant state as claimed);

at least one transceiver for at least one of transmission and reception of data signals; and (Eisele, col. 4, lines 52-55, "At least in stations which not only are capable of receiving but also of transmitting data each line is coupled, via an associated switch,") where associated switch can a "transceiver for transmission and reception of data signals" as claimed;

at least one fault identification device configured to: (Eisele, fig. 2 ,element 26 and 27, col. 6, lines 39-42, "The line 31 is also connected to two fault detection circuits 26 and 27 ") where fault detection circuit can be "fault identification device" as claimed.

cause the one of said bus subscribers to be able to assume a recessive state and the dominant state (Eisele, col. 6, lines 17-21***),***

make available an internal high potential and an internal low potential in the one of said bus subscribers (Eisele, col. 6, lines 15-16, "the line 11 carries a high potential and the line 12 carries a low potential.");

carry out a check for line faults by comparing voltage levels on the bus lines with threshold values related to one of an internal high level and an internal low level of the one of said bus subscribers (Eisele, fig. 2, col. 6, lines 28-51)***;***

Eisele does not specifically discloses ***a check for a line fault only when the at least one of the said bus subscribers is placed in said dominant state by said switching state of said switches;***

However, Williamson discloses the above claim limitations, (Fig. 6, element 614, 615, Col. 5, lines 1-9, where first and second pinned fault detection means checks for fault (short circuit) in the dominant state);

Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Williamson's diagnostic method to Eisele's teaching because one of the ordinary skill in the art would have been motivated to provide fault tolerant serial communications in a network (Williamson, Col. 2, lines 26-27).

As per claim 19, claim 18 is incorporated and Eisele further comprising at least one fault detection device comparing at least one voltage level on one of said bus lines with a threshold value related to one of the internal low level and the internal high level and providing a fault signal. (Eisele, fig. 3, col. 2, lines 10-27, "a comparator which forms not only the difference between the potentials on the two lines but also compares this difference with a given first threshold value, the transmitted data signal..... each line is connected to a low potential or a high potential via a resistor", col. 8, lines 23-26, "A fault signal is thus generated on the corresponding line 36a or 36b").

Claim 25 has similar limitations as claim 19 and therefore is rejected under the same reasons set forth in rejections of claim 19 and further ***means for detecting*** can be fault detection circuit (Eisele, fig. 2, element 27 and 26) ***means for comparing*** can be a comparator (Eisele, fig. 2, element 21).

As per claim 20, claim 19 is incorporated and Eisele further discloses:
wherein said at least one fault detection device is:
a first fault detection device comparing a voltage level on one of said data lines with a first threshold value and provision a first fault signal; and (Eisele, col. 6, lines 29-59, "it subtracts the potential on the line 12 from that on the line 11 and compares the difference of correct sign with a first threshold value….generates a signal on the line 34..") where voltage difference in line potentials can be "a voltage level on one of said data lines" as claimed. Line 34 is connected to the lower fault detection circuit 27;
a second fault detection device comparing a voltage level on the other one of said data lines with a second threshold value and providing a second fault signal. (Eisele, col. 2, lines 36-46, "a second comparator which is coupled to the first line in order to generate an output signal of the first value on a second comparator output if the potential on the first line exceeds a second threshold value", col. 7, lines 12-15, "The upper fault detection circuit 26 generates a fault signal on an output line 36a").

Claim 26 has similar limitations as claim 20 and therefore is rejected under the same reasons set forth in rejections of claim 20 and further ***means for detection*** can be fault detection circuit (Eisele, fig. 2, element 27 and 26) ***means for comparing*** can be a comparator (Eisele, fig. 2, element 21).

As per claim 21, claim 20 is incorporated and Eisele further comprising a first data detection device for detection of transmitted data, said first data detection device comparing voltage levels on said bus lines and providing a first data signal. (Eisele, col. 2, lines 10-27, "a comparator which forms not only the difference between the potentials on the two lines but also compares this difference with a given first threshold value, the transmitted data signal..... each line is connected to a low potential or a high potential via a resistor") where voltage difference in line potentials can be "a voltage level on one of said data lines" as claimed and one of the two lines interrupted means "fault detected" as claimed.

Claim 27 has similar limitations as claim 21 and therefore is rejected under the same reasons set forth in rejections of claim 21 and further ***means for detection*** can be fault detection circuit (Eisele, fig. 2, element 27 and 26) ***means for comparing*** can be a comparator (Eisele, fig. 2, element 21).

As per claim 22, claim 21 is incorporated and Eisele further comprising: at least one second data detection device for detection of transmitted data, said second data detection device comparing a voltage level on at least one of said data lines with at least one threshold value related to the internal low level to provide at least one second data signal; and (Eisele, col. 2, lines 36-46, "a second comparator which is coupled to the first line in order to generate an output signal of the first value on a second comparator output if the potential on the first line exceeds a second threshold value", col. 7, lines 12-15, "The upper fault detection circuit 26 generates a fault signal on an output line 36a");

a switch switching between said first data signal and said at least one second data signal as a function of said at least one fault signal. (Eisele, col. 2, lines 35-46, "a second comparator which is coupled to the first line in order to generate an output signal of the first value on a second comparator output if the potential on the first line exceeds a second threshold value .....memory being coupled to a switch for switching the data output from the first comparator output to the second comparator output") where second comparator generates a fault signal as claimed.

Claim 28 has similar limitations as claim 22 and therefore is rejected under the same reasons set forth in rejections of claim 22 and further ***means for detection*** can be fault detection circuit (Eisele, fig. 2, element 27 and 26) ***means for***

comparing can be a comparator (Eisele, fig. 2, element 21). And a ***means for switching*** can be a switch (Eisele, fig. 1, element 5).

As per claim 30, a bus system, comprising:

a data bus having at least two bus lines; and (Eisele, fig 1, bus lines 11, 12 and 13, col. 3, lines 2-5, col. 5, lines 58-60, "three lines 11, 12 and 13");

at least two bus subscribers coupled to said data bus for serial data transfer of binary data between said bus subscribers, at least one of said bus subscribers configured (Eisele, fig 1, stations 1, 2 and 3, col. 5, lines 58-64, "three stations 1, 2 and 3 which are interconnected via three lines 11, 12 and 13....the data is transmitted") where station can be "bus subscriber" as claimed;

to assume a recessive state and a dominant state and having (Eisele, col. 6, lines 16-21, "in the case of open switches 6 and 7, therefore, will be referred to as the recessive state hereinafter and the state in the case of closed switches 6 and 7 as the dominant state.");

internal high and low potentials; (Eisele, col. 6, lines 15-16, "the line 11 carries a high potential and the line 12 carries a low potential.");

internal high and low levels; (Eisele, col. 6, lines 22-27);

at least one control unit; (Eisele, fig 1, element 5, col. 6, lines 5-15, "the station 2 comprises a control device 5") where control device can be "control unit" as claimed;

Switches for assuming a switching state placing the one of said bus subscribers in a dominant state; (Eisele, col. 6, lines 17-21, "the state in the case of closed switches 6 and 7 as the dominant state.", where switches are used to place bus subscribers in recessive or dominant state as claimed);

at least one transceiver for at least one of transmission and reception of data signals, said transceiver connected to said control unit; and Eisele, col. 4, lines 52-55, "At least in stations which not only are capable of receiving but also of transmitting data each line is coupled, via an associated switch,") where associated switch can a "transceiver for transmission and reception of data signals" as claimed;

at least one fault identification device connected to at least said transceiver and carrying out: (Eisele, fig. 2 ,element 26 and 27, col. 6, lines 39-42, "The line 31 is also connected to two fault detection circuits 26 and 27 ") where fault detection circuit can be "fault identification device" as claimed;

a check for line faults by comparing voltage levels on said bus lines with threshold values related to one of said internal high level and said internal low level. (Eisele, fig. 2, col. 6, lines 28-51, "The line 11 is also connected to a comparator 22 which compares the potential on this line with a threshold value which is valued, taking into account tolerances, between the dominant and the

recessive potential on the line 11. The comparator 22 generates a high signal on the line 32 if the potential on the line 11 exceeds the threshold value.");

Eisele does not specifically discloses ***a check for a line fault only when the at least one of the said bus subscribers is placed in said dominant state by said switching state of said switches;***

However, Williamson discloses the above claim limitations, (Fig. 6, element 614, 615, Col. 5, lines 1-9, where first and second pinned fault detection means checks for fault (short circuit) in the dominant state);

Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Williamson's diagnostic method to Eisele's teaching because one of the ordinary skill in the art would have been motivated to provide fault tolerant serial communications in a network (Williamson, Col. 2, lines 26-27).

7. ***Claim 23*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Eisele and Williamson in view of Barclay et al (U. S. Patent No. 4,516,248 referred herein after Barclay)

As per claim 23, claim 18 is incorporated and Eisele further discloses:

wherein said data bus serially transmits binary data and is in the form of a differential, (Eisele, col. 5, lines 58-64)

Eisele does not specifically disclose:

Said data bus transmits duplex signals with two-wire data bus having two bus lines twisted with one another.

However, in the analogous art Barclay discloses:

Said data bus transmits serially by duplex signals with two-wire data bus having two bus lines twisted with one another. (Barclay, fig. 3, lines 58 and 60, col. 10, lines 54-55, "Twisted pair wire is the least expensive means of data transmission", col. 7, lines 62-65, "the user interface circuit 30 is full duplex"). Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Barclay's data transmission method to Eisele's and Williamson's teaching because one of the ordinary skill in the art would have been motivated to a high performance data communication peer network. (Barclay, col. 1, lines 7-8).

9. ***Claim 24*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Eisele and Williamson in view of Baker (U. S. Patent No. 6,535,028).

As per claim 24, claim 18 is incorporated and Eisele does not specifically disclose***: wherein the bus system is a CAN bus system.***

However, Baker discloses: ***the bus system is a CAN bus system***. (Baker, col. 1, lines 6-8, "circuit for a differential serial bus, such as a CAN ("Controller Area Network") bus system."

Therefore it would have been obvious to the one of ordinary skill in the art at the time of invention to incorporate Baker's bus system to Eisele's and Williamson's teaching because one of the ordinary skill in the art would have been motivated to operate in noisy electrical environments with a high level of data integrity, and its open architecture and user-definable transmission medium make it extremely flexible. (Baker, col. 1, lines 12-15).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAMINI PATEL whose telephone number is (571)270-3902. The examiner can normally be reached on Monday to Thursday,6am-4:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on 571-272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114

/Kamini Patel/
Examiner, Art Unit 2114